Features

• 240pin, unbuffered dual in-line memory module (UDIMM)
• Fast data transfer rates: PC2-4200, PC3-5300, PC3-6400
• Single or Dual rank
• 512MB (64Meg x 64), 1GB(128 Meg x 64), 2GB (256 Meg x 64)
• JEDEC standard 1.8V I/O (SSTL_18-compatible)
• V_{DD} = V_{DDQ} = 1.8V ±0.1V
• V_{DDSPD} = 3.0V to 3.6V
• Differential clock inputs, Differential data strobe (DQS, DQS#) option
• 4*n*-bit prefetch architecture
• Multiple internal device banks for concurrent operation
• Programmable CAS latency (CL)
• Posted CAS additive latency (AL)
• WRITE latency = READ latency - 1 tCK
• Programmable burst lengths (BL): 4 or 8
• Adjustable data-output drive strength
• 64ms, 8,192-cycle refresh
• On-die termination (ODT)• Serial presence-detect (SPD) EEPROM
• Gold edge contacts
• Pb-free

Module Specification

Part Number	Module Density & Configuration	Bandwidth	Data Rate	Timing (tCL-tRCD-tRP)
SP512MBLRU533O01(2)	512MB (64Mx64) 64Mx8 1Rank	PC2-4200	DDR2-533	4-4-4
SP512MBLRU667O01(2)		PC2-5300	DDR2-667	5-5-5
SP512MBLRU800O01(2)		PC2-6400	DDR2-800	5-5-5
SP001GBLRU533O01(2)	1GB (128Mx64) 64Mx8 2Ranks	PC2-4200	DDR2-533	4-4-4
SP001GBLRU667O01(2)		PC2-5300	DDR2-667	5-5-5
SP001GBLRU800O01(2)		PC2-6400	DDR2-800	5-5-5
SP001GBLRU533S01(2)	1GB (128Mx64) 128Mx8 1Rank	PC2-4200	DDR2-533	4-4-4
SP001GBLRU667S01(2)		PC2-5300	DDR2-667	5-5-5
SP001GBLRU800S01(2)		PC2-6400	DDR2-800	5-5-5
SP002GBLRU533S02	2GB (256Mx64) 128Mx8 2Rank	PC2-4200	DDR2-533	4-4-4
SP002GBLRU667S01(2)		PC2-5300	DDR2-667	5-5-5
SP002GBLRU800S01(2)		PC2-6400	DDR2-800	5-5-5
SP001GBLRU667O21(2)	512MBx2 Kit Package	PC2-5300	DDR2-667	5-5-5
SP001GBLRU800O21(2)		PC2-6400	DDR2-800	5-5-5
SP002GBLRU667O21(2)	1GBx2 Kit Package	PC2-5300	DDR2-667	5-5-5
SP002GBLRU800O21(2)		PC2-6400	DDR2-800	5-5-5
SP002GBLRU667S2(2)	1GBx2 Kit Package	PC2-5300	DDR2-667	5-5-5
SP002GBLRU800S2(2)		PC2-6400	DDR2-800	5-5-5
SP004GBLRU800S22	2GBx2 Kit Package	PC2-6400	DDR2-800	5-5-5

Note:

1. This document supports all LRU Series DDR2 240Pin UDIMM products.
2. Some item was being EOL in this list, Please contact with our sales Dep.
3. All part numbers end with a double-digit code is for customize use only.
   Example: SP512MBLRU533O02-XX

Pin Assignments

240-Pin UDIMM Front							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	VREF	31	DQ19	61	A4	91	VSS
2	VSS	32	VSS	62	VDDQ	92	DQS5#
3	DQ0	33	DQ24	63	A2	93	DQS5
4	DQ1	34	DQ25	64	VDD	94	VSS
5	VSS	35	VSS	65	VSS	95	DQ42
6	DQS0#	36	DQS3#	66	VSS	96	DQ43
7	DQS0	37	DQS3	67	VDD	97	VSS
8	VSS	38	VSS	68	NC	98	DQ48
9	DQ2	39	DQ26	69	VDD	99	DQ49
10	DQ3	40	DQ27	70	A10	100	VSS
11	VSS	41	VSS	71	BA0	101	SA2
12	DQ8	42	NC	64	VDDQ	102	NC
13	DQ9	43	NC	73	WE#	103	VSS
14	VSS	44	VSS	74	CAS#	104	DQS6#
15	DQS1#	45	NC	75	VDDQ	105	DQS6
16	DQS1	46	NC	76	S1	106	VSS
17	VSS	47	VSS	77	ODT1	107	DQ50
18	NC	48	NC	78	VDDQ	108	DQ51
19	NC	49	NC	79	VSS	109	VSS
20	VSS	50	Vss	80	DQ32	110	DQ56
21	DQ10	51	VDDQ	81	DQ33	111	DQ57
22	DQ11	52	CKE0	82	VSS	112	VSS
23	VSS	53	VDD	83	DQS4#	113	DQS7#
24	DQ16	541	NC/BA2	84	DQS4	114	DQS7
25	DQ17	55	NC	85	VSS	115	VSS
26	VSS	56	VDDQ	86	DQ34	116	DQ58
27	DQS2#	57	A11	87	DQ35	117	DQ59
28	DQS2	58	A7	88	VSS	118	VSS
29	VSS	59	VDD	89	DQ40	119	SDA
30	DQ18	60	A5	90	DQ41	120	SCL

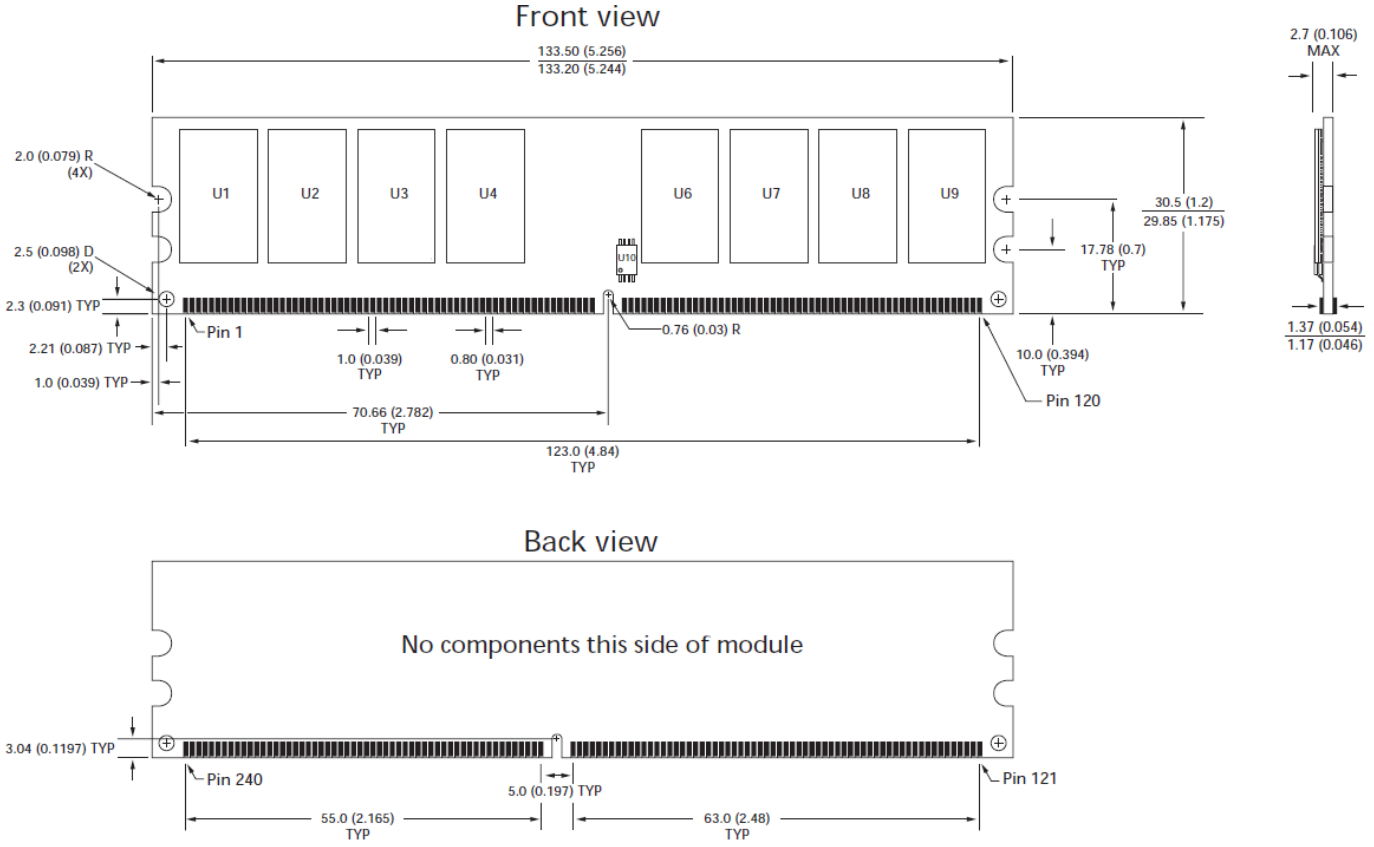
240-Pin UDIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
121	VSS	151	VSS	181	VDDQ	211	DM5
122	DQ4	152	DQ28	182	A3	212	NC
123	DQ5	153	DQ29	183	A1	213	VSS
124	VSS	154	VSS	184	VDD	214	DQ46
125	DM0	155	DM3	185	CK0	215	DQ47
126	NC	156	NC	186	CK0#	216	VSS
127	VSS	157	VSS	187	VDD	217	DQ52
128	DQ6	158	DQ30	188	A0	218	DQ53
129	DQ7	159	DQ31	189	VDD	219	VSS
130	VSS	160	VSS	190	BA1	220	CK2
131	DQ12	161	NC	191	VDDQ	221	CK2#
132	DQ13	162	NC	192	RAS#	222	VSS
133	VSS	163	VSS	193	S0#	223	DM6
134	DM1	164	NC	194	VDDQ	224	NC
135	NC	165	NC	195	ODT0	225	VSS
136	VSS	166	VSS	196	NC/A13	226	DQ54
137	CK1	167	NC	197	VDD	227	DQ55
138	CK1#	168	NC	198	VSS	228	VSS
139	VSS	169	Vss	199	DQ36	229	DQ60
140	DQ14	170	VDDQ	200	DQ37	230	DQ61
141	DQ15	171	CKE1	201	VSS	231	VSS
142	VSS	164	VDD	202	DM4	232	DM7
143	DQ20	173	NC	203	NC	233	NC
144	DQ21	174	NC	204	VSS	234	VSS
145	VSS	175	VDDQ	205	DQ38	235	DQ62
146	DM2	176	A12	206	DQ39	236	DQ63
147	NC	177	A9	207	VSS	237	VSS
148	VSS	178	VDD	208	DQ44	238	VDDSPD
149	DQ22	179	A8	209	DQ45	239	SA0
150	DQ23	180	A6	210	VSS	240	SA1

Pin Description

Symbol	Type	Description
A0–A13	Input (SSTL_18)	**Address inputs:** Provide the row address for ACTIVE commands, and the column address and auto precharge bit (A10) for READ/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one device bank (A10 LOW, device bank selected by BA0–BA2) or all device banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command. A0–A12 (256MB) and A0–A13 (512MB, 1GB).
BA0–BA2	Input (SSTL_18)	**Bank address inputs:** BA0–BA2 define to which device bank an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA0–BA2 define which mode register, including MR, EMR, EMR(2), and EMR(3), is loaded during the LOAD MODE command. BA0, BA1 (256MB, 512MB) and BA0–BA2 (1GB).
CK0, CK0#, CK1, CK1#, CK2, CK2#	Input (SSTL_18)	**Clock:** CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and the negative edge of CK#. Output data (DQs and DQS/DQS#) is referenced to the crossings of CK and CK#.
CKE0 ,CKE1	Input (SSTL_18)	**Clock enable:** CKE (registered HIGH) activates and CKE (registered LOW) deactivates clocking circuitry on the DDR2 SDRAM.
ODT0, ODT1	Input (SSTL_18)	**On-die termination:** ODT (registered HIGH) enables termination resistance internal to the DDR2 SDRAM. When enabled, ODT is only applied to the following pins: DQ, DQS, DQS#, and CB. The ODT input will be ignored if disabled via the LOAD MODE command.
RAS#, CAS#, WE#	Input (SSTL_18)	**Command inputs:** RAS#, CAS#, and WE# (along with S#) define the command being entered.
S0#, S1#	Input (SSTL_18)	**Chip select:** S# enables (registered LOW) and disables (registered HIGH) the command decoder.
SA0–SA2	Input (SSTL_18)	**Presence-detect address inputs:** These pins are used to configure the presence-detect devices.
SCL	Input (SSTL_18)	**Serial clock for presence-detect:** SCL is used to synchronize the presence-detect data transfer to and from the module.
SDA	I/O	**Serial presence-detect data:** SDA is a bidirectional pin used to transfer addresses and data into and out of the presence-detect portion of the module.
DM0–DM7	I/O (SSTL_18)	**Data input mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH, along with that input data, during a write access. DM is sampled on both edges of DQS. Although DM pins are input-only, the DM loading is designed to match that of DQ and DQS pins.
DQ0–DQ63	I/O (SSTL_18)	**Data input/output:** Bidirectional data bus.
DQS0–DQS7, DQS0#–DQS7#	I/O (SSTL_18)	**Data strobe:** Output with read data, input with write data for source synchronous operation. Edge-aligned with read data, center-aligned with write data. DQS# is only used when differential data strobe mode is enabled via the LOAD MODE command.
V_{DD}/V_{DDQ}	Supply	**Power supply:** 1.8V ±0.1V.
V_{DDSPD}	Supply	**Serial EEPROM positive power supply:** +1.7V to +3.6V.
V_{REF}	Supply	SSTL_18 reference voltage. ($V_{DD}/2$)
V_{SS}	Supply	Ground.
NC	–	**No connect:** These pins are not connected on the module.

Simplified Mechanical Drawing(x8 1Rank)

X64 DIMM, populated as one physical rank of x8 DDR2 SDRAMs

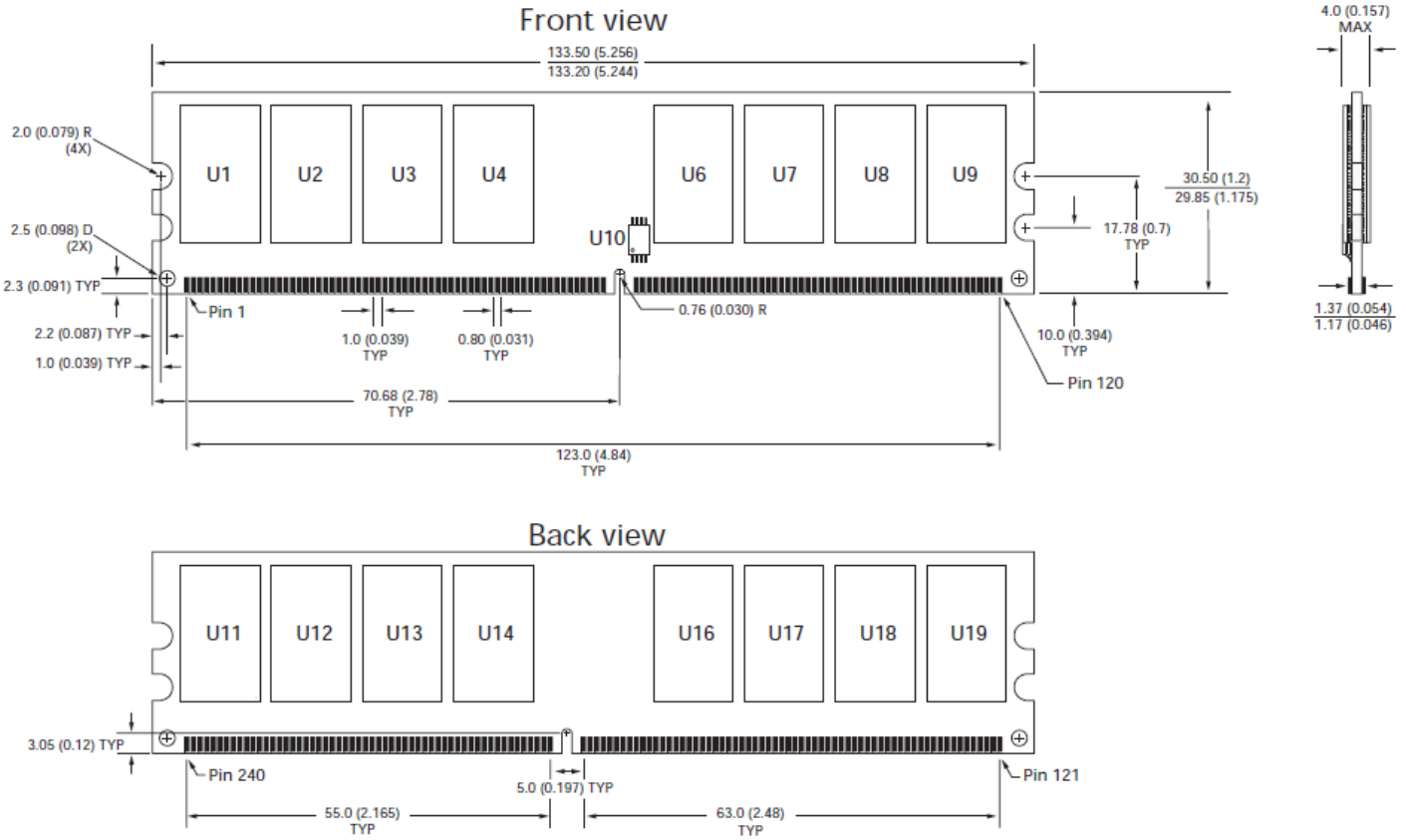


Note: 1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.

Note: 2. The dimensional diagram is for reference only.

Simplified Mechanical Drawing(x8 2Ranks)

X64 DIMM, populated as one physical rank of x8 DDR2 SDRAMs



Note: 1. All dimensions are in millimeters (inches); MAX/MIN or typical (TYP) where noted.

Note: 2. The dimensional diagram is for reference only.