1. Description

The SP512MBRDE333O01 is a 64M x 8bits Double Data Rate SDRAM high-density for DDR-333.The SP512MBRDE333O01 consists of 8pcs CMOS 64x8 bits Double Data Rate SDRAMs in 66 pin TSOP package, and a 2048 bits serial EEPROM on a 184-pin printed circuit board. The SP512MBRDE333O01 is a Dual In-Line Memory Module and is intended for mounting into 184-pin connector sockets. Synchronous design allows precise cycle control with the use of system clock. Data I/O transactions are possible on both edges of DQS. Range of operation frequencies, programmable latencies allow the same device to be useful for a variety of high bandwidth, high performance memory system applications.

2. Features

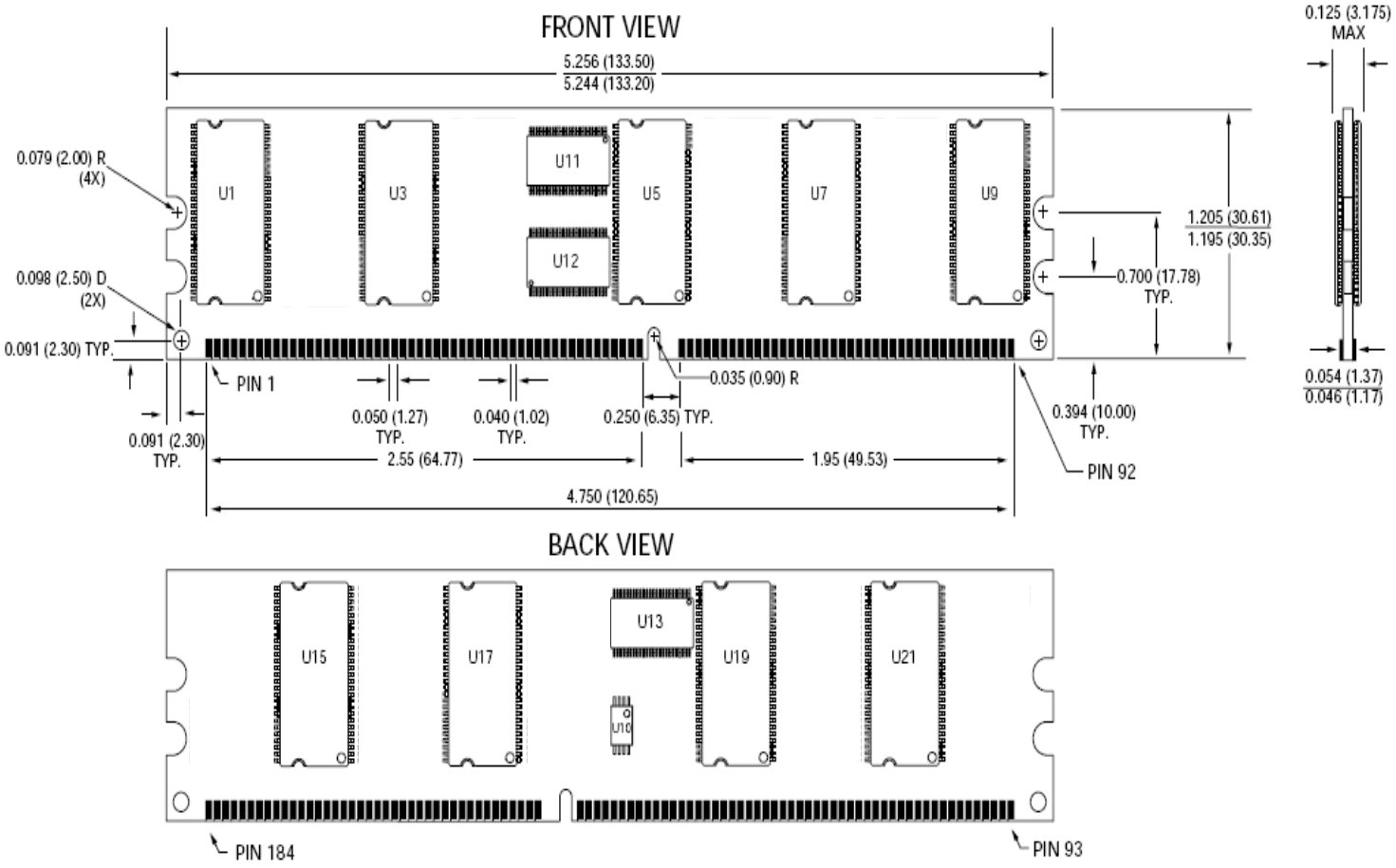
- **Double--data--rate architecture; two data transfers per clock cycle**
- **Bidirectional, data strobe (DQS) is transmitted/received with data, to be used in capturing data at the receiver**
- **DQS is edge--aligned with data for READs; center--aligned with data for WRITEs**
- **Differential clock inputs (CK and /CK)**
- **DLL aligns DQ and DQS transitions with CK transitions**
- **Commands entered on each positive CK edge; data and data mask referenced to both edges of DQS**
- **Four internal banks for concurrent operation**
- **Registered inputs with one-clock delay**
- **Phase-lock loop (PLL) clock driver to reduce loading**
- **Supports ECC error detection and correction**
- **Data mask (DM) for write data**
- **Burst lengths: 2, 4, or 8**
- **AUTOPRECHARGE option for each burst access**
- **Auto Refresh and Self Refresh Modes**
- **JEDEC standard 2.5 V (SSTL_2 compatible) I/O**
- **66pin TSOP II Leaded & Pb-Free (RoHS compliant) package**

This document is a general product description and is subject to change without notice

3. Module Specification

Item	Specification
Capacity	512MByte
Physical Bank(s)	1
Module Organization	64M x 72bit
Module Type	Registered
Speed Grade	PC-2700 / (DDR333)
Voltage Interface	SSTL_2
Power Supply Voltage	2.5V ±0.2V
Burst Lengths	2,4,8
DRAM Organization	64M x 8bit DDR SDRAM
PCB Layer	6Layers
Contact Tab	184pin GOLD Flash Plating
Serial PD	Support

4. Simplified Mechanical Drawing with Keying Positions



Notes **：** 1. All dimensions are in inches (millimeters); MAX/MIN or typical (TYP) where noted.

5. Pinouts

Pin Num	Pin Name	Pin Num	Pin Name	Pin Num	Pin Name	Pin Num	Pin Name	Pin Num	Pin Name	Pin Num	Pin Name	Pin Num	Pin Name	Pin Num	Pin Name
01	VREF	**24**	DQ17	**47**	DQS8	**70**	VDD	**93**	VSS	**116**	VSS	**139**	VSS	**162**	DQ47
02	DQ0	**25**	DQS2	**48**	A0	**71**	NC	**94**	DQ4	**117**	DQ21	**140**	DM8	**163**	NC
03	VSS	**26**	VSS	**49**	CB2	**72**	DQ48	**95**	DQ5	**118**	A11	**141**	A10	**164**	VDDQ
04	DQ1	**27**	A9	**50**	VSS	**73**	DQ49	**96**	VDDQ	**119**	DM2	**142**	CB6	**165**	DQ52
05	DQS0	**28**	DQ18	**51**	CB3	**74**	VSS	**97**	DM0	**120**	VDD	**143**	VDDQ	**166**	DQ53
06	DQ2	**29**	A7	**52**	BA1	**75**	*/CK2	**98**	DQ6	**121**	DQ22	**144**	CB7	**167**	NC/A13
07	VDD	**30**	VDDQ	**53**	DQ32	**76**	*CK2	**99**	DQ7	**122**	A8	**145**	VSS	**168**	VDD
08	DQ3	**31**	DQ19	**54**	VDDQ	**77**	VDDQ	**100**	VSS	**123**	DQ23	**146**	DQ36	**169**	DM6
09	NC	**32**	A5	**55**	DQ33	**78**	DQS6	**101**	NC	**124**	VSS	**147**	DQ37	**170**	DQ54
10	/RESET	**33**	DQ24	**56**	DQS4	**79**	DQ50	**102**	NC	**125**	A6	**148**	VDD	**171**	DQ55
11	VSS	**34**	VSS	**57**	DQ34	**80**	DQ51	**103**	NC	**126**	DQ28	**149**	DM4	**172**	VDDQ
12	DQ8	**35**	DQ25	**58**	VSS	**81**	VSS	**104**	VDDQ	**127**	DQ29	**150**	DQ38	**173**	NC
13	DQ9	**36**	DQS3	**59**	BA0	**82**	VDDID	**105**	DQ12	**128**	VDDQ	**151**	DQ39	**174**	DQ60
14	DQS1	**37**	A4	**60**	DQ35	**83**	DQ56	**106**	DQ13	**129**	DM3	**152**	VSS	**175**	DQ61
15	VDDQ	**38**	VDD	**61**	DQ40	**84**	DQ57	**107**	DM1	**130**	A3	**153**	DQ44	**176**	VSS
16	*CK1	**39**	DQ26	**62**	VDDQ	**85**	VDD	**108**	VDD	**131**	DQ30	**154**	/RAS	**177**	DM7
17	*/CK1	**40**	DQ27	**63**	/WE	**86**	DQS7	**109**	DQ14	**132**	VSS	**155**	DQ45	**178**	DQ62
18	VSS	**41**	A2	**64**	DQ41	**87**	DQ58	**110**	DQ15	**133**	DQ31	**156**	VDDQ	**179**	DQ63
19	DQ10	**42**	VSS	**65**	/CAS	**88**	DQ59	**111**	CKE1	**134**	CB4	**157**	/S0	**180**	VDDQ
20	DQ11	**43**	A1	**66**	VSS	**89**	VSS	**112**	VDDQ	**135**	CB5	**158**	/S1	**181**	SA0
21	CKE0	**44**	CB0	**67**	DQS5	**90**	NC	**113**	*BA2	**136**	VDDQ	**159**	DM5	**182**	SA1
22	VDDQ	**45**	CB1	**68**	DQ42	**91**	SDA	**114**	DQ20	**137**	CK0	**160**	VSS	**183**	SA2
23	DQ16	**46**	VDD	**69**	DQ43	**92**	SCL	**115**	NC/A12	**138**	/CK0	**161**	DQ46	**184**	VDDSPD

NOTE **：** 1. * : These pins are not used in this module.
2. Pin 115 is No Connect for 256MB, or A12 for 512MB and 1GB.
3. Pin 167 is NC for 256MB, 512MB, and 1GB, or A13 for 2GB.

6. Pin Description

SYMBOL	TYPE	DESCRIPTION
CK, /CK	Input	**Clock:** CK and /CK are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of /CK. Output data (DQs and DQS /DQS) is referenced to the crossings of CK and /CK.
/RAS, /CAS, /WE	Input	**Command Inputs:** /RAS, /CAS and /WE (along with /S) define the command being entered.
CKE	Input	**Clock Enable:** CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is synchronous for power down entry and exit, and for self refresh entry. CKE is asynchronous for self refresh exit. CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, CK, and CKE are disabled during power-down. Input buffers, excluding CKE, are disabled during self refresh.
/S0-/S1	Input	**Chip Select:** Enables the associated SDRAM command decoder when low and disables the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue. Rank 0 is selected by S0; Rank 1 is selected by S1
DM0-DM8	Input	**Input Data Mask:** DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS. Although DM pins are input only, the DM loading matches the DQ and DQS loading. For x8 device, the function of DM or RDQS/RDQS is enabled by EMRS command.
BA0 - BA2	Input	**Bank Address Inputs:** BA0 and BA1 for 256 and 512Mb, BA0 - BA2 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines if the mode register or extended mode register is to be accessed during a MRS or EMRS cycle.
A0 - A12	Input	**Address Inputs:** Provided the row address for Active commands and the column address and Auto Precharge bit for Read/Write commands, to select one location out of the memory array in the respective bank. A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by BA0, BA1. The address inputs also provide the op-code during Mode Register Set commands.
DQ0-DQ63	Input/Output	**Data bit Input/ Output:** Bi-directional data bus.
CB0-CB7	Input/Output	ECC check bits.
DQS0-DQS8	Input/Output	**Data Strobe:** output with read data, input with write data for source-synchronous operation. Edge-aligned with read data, center-aligned with write data. For Rawcards using x16 orginized DRAMs DQ0-7 connect to the LDQS pin of the DRAMs and DQ8-17 connect to the UDQS pin of the DRAM.
NC		**No Connect:** No internal electrical connection is present.
V_{DDQ}	Supply	Power supplies for the DDR SDRAM output buffers to provide improved noise immunity. For all current DDR unbuffered DIMM designs, V_{DDQ} shares the same power plane as V_{DD} pins
V_{DD}, V_{SS}	Supply	Power and ground for the DDR SDRAM input buffers, and core logic. V_{DD} and V_{DDQ} pins are tied to V_{DD} / V_{DDQ} planes on these modules.
V_{REF}	Supply	Reference voltage for SSTL_2 inputs.
SDA	Input/Output	This bidirectional pin is used to transfer data into or out of the SPD EEPROM. A resistor must be connected from the SDA bus line to V_{DD} to act as a pullup on the system board.
SCL	Input	This signal is used to clock data into and out of the SPD EEPROM. A resistor may be connected from the SCL bus time to V_{DD} to act as a pullup on the system board.
V_{DD}SPD	Supply	Power supply for SPD EEPROM. This supply is separate from the V_{DD} / V_{DDQ} power plane. EEPROM supply is operable from 1.7V to 3.6V.
SA0-SA2	Input	These signals and tied at the system planar to either VSS or VDD to configure the serial SPD EERPOM address range.
/RESET	Input	The /RESET pin is connected to the /RST pin on the register and to the OE pin on the PLL. When low, all register outputs will be driven low and the PLL clocks to the DRAMs and register(s) will be set to low level (The PLL will remain synchronized with the input clock.